

Fig. 1

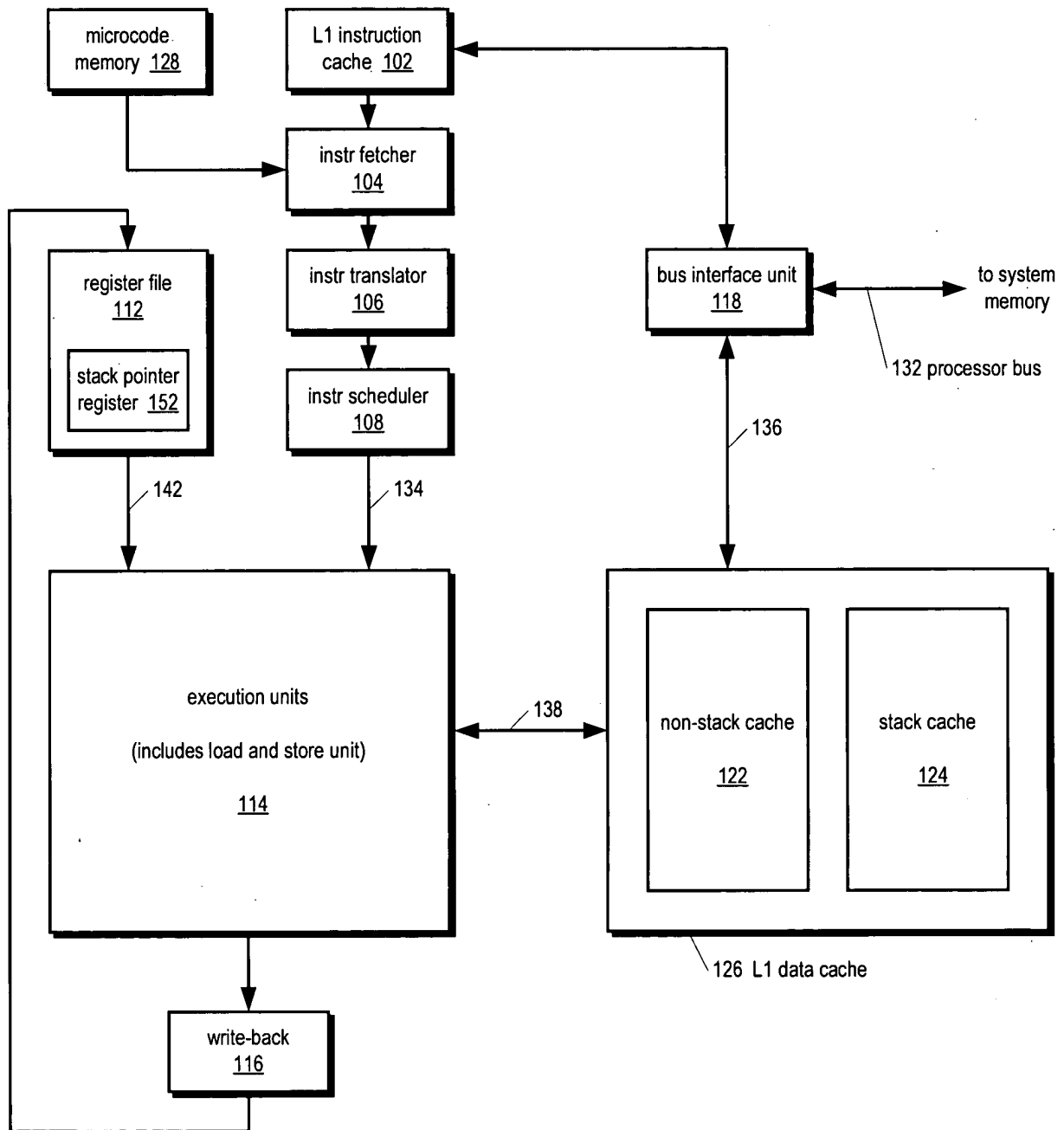
Microprocessor

Fig. 2

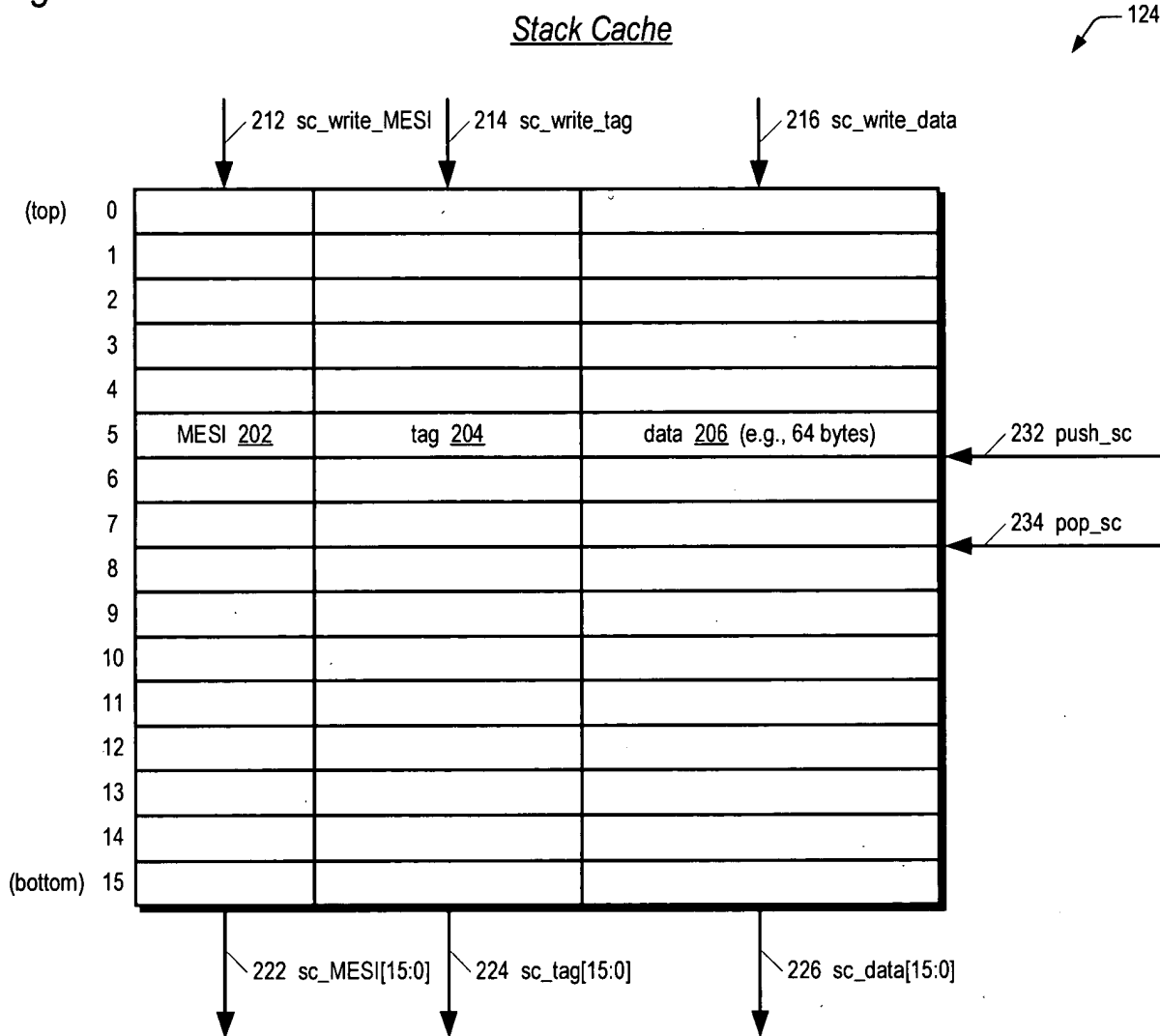


Fig. 3

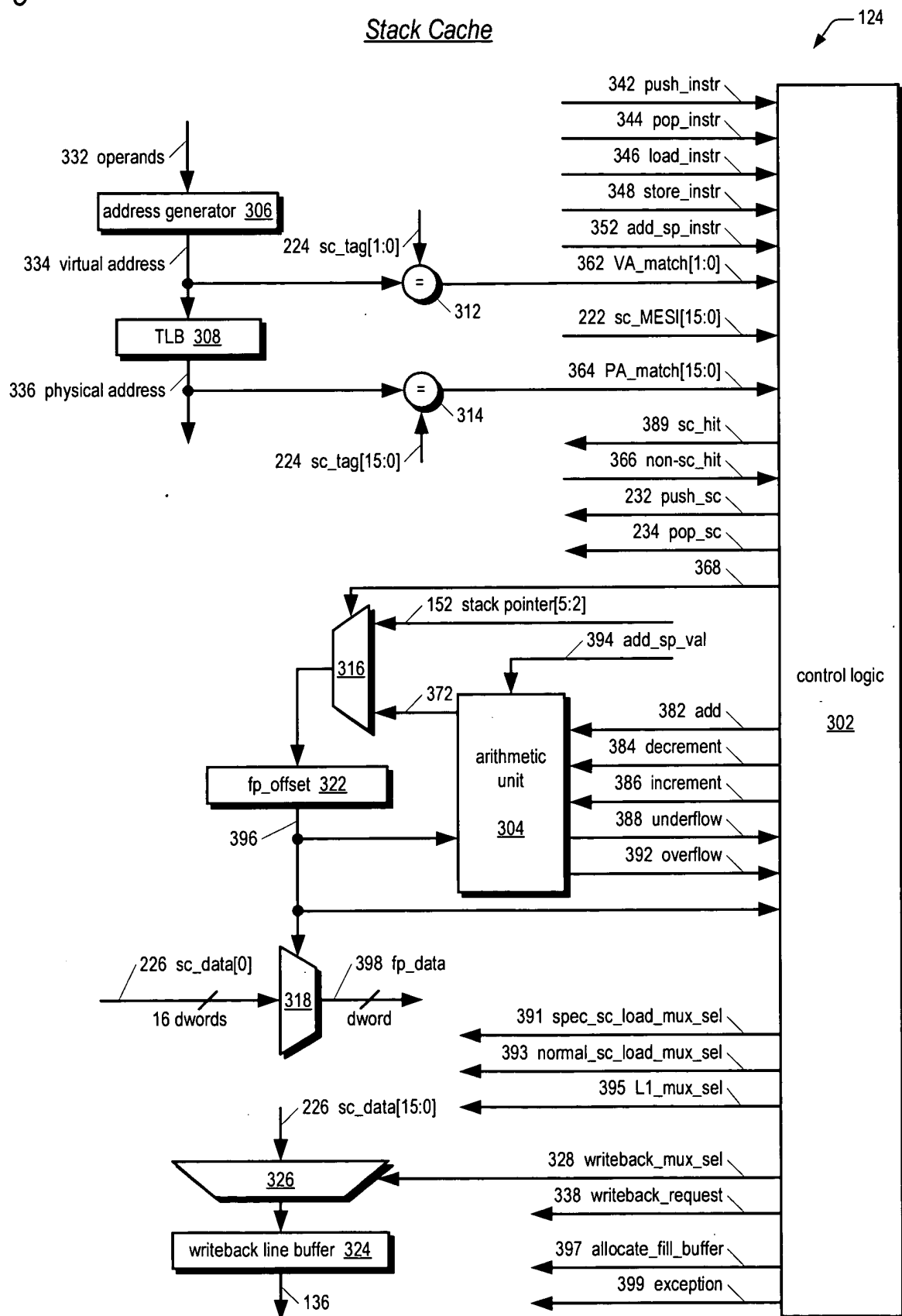
Stack Cache

Fig. 4

L1 Data Cache

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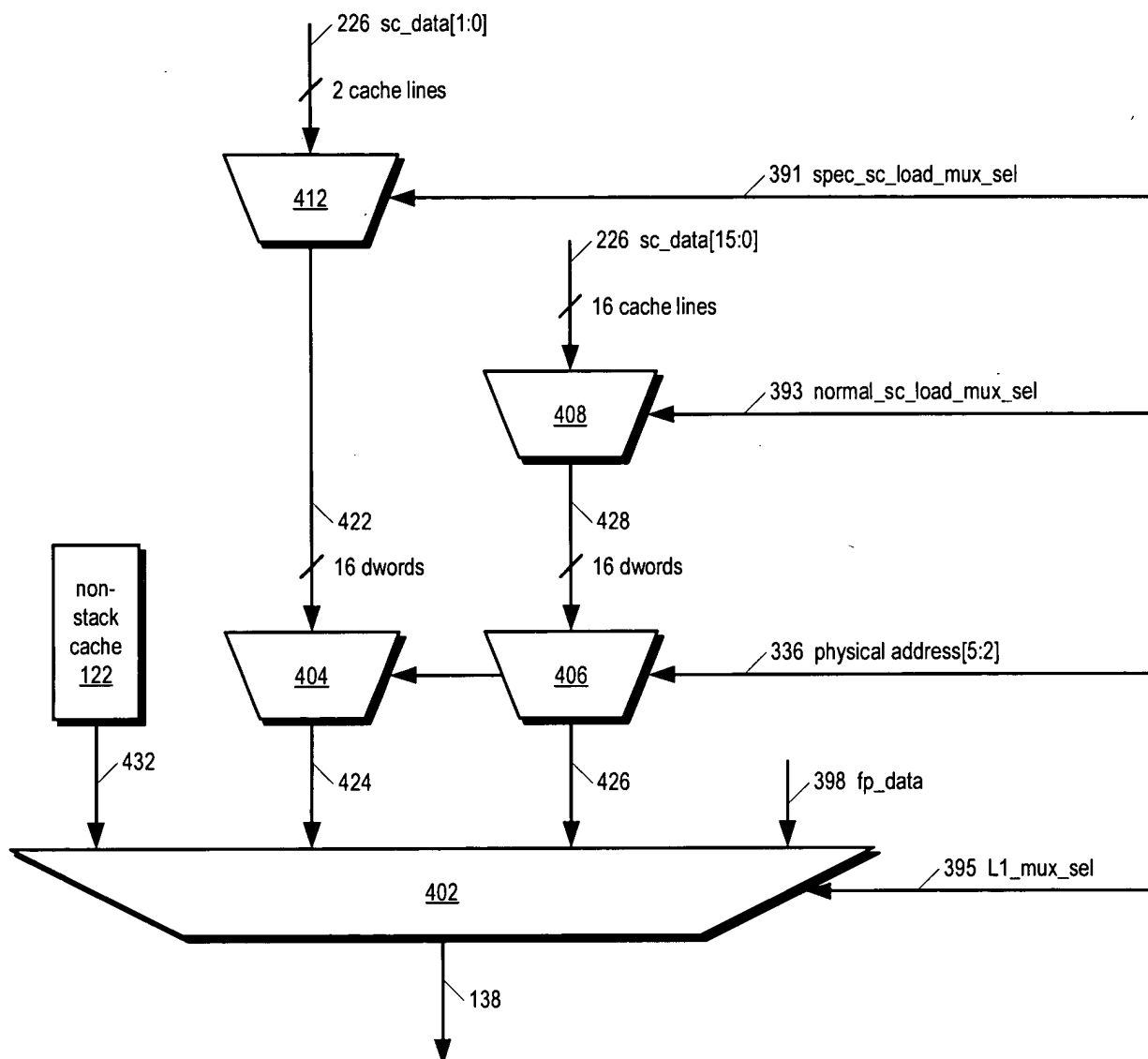


Fig. 5

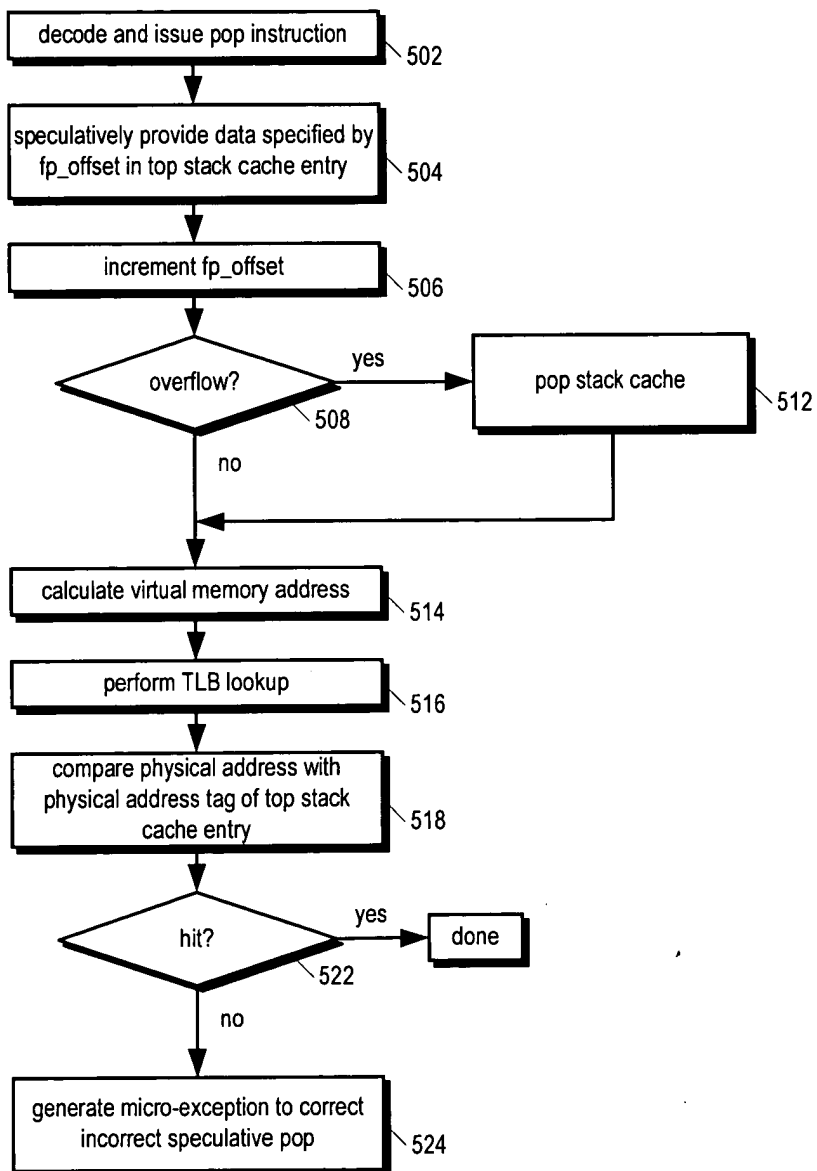
Fast Pop Operation

Fig. 6

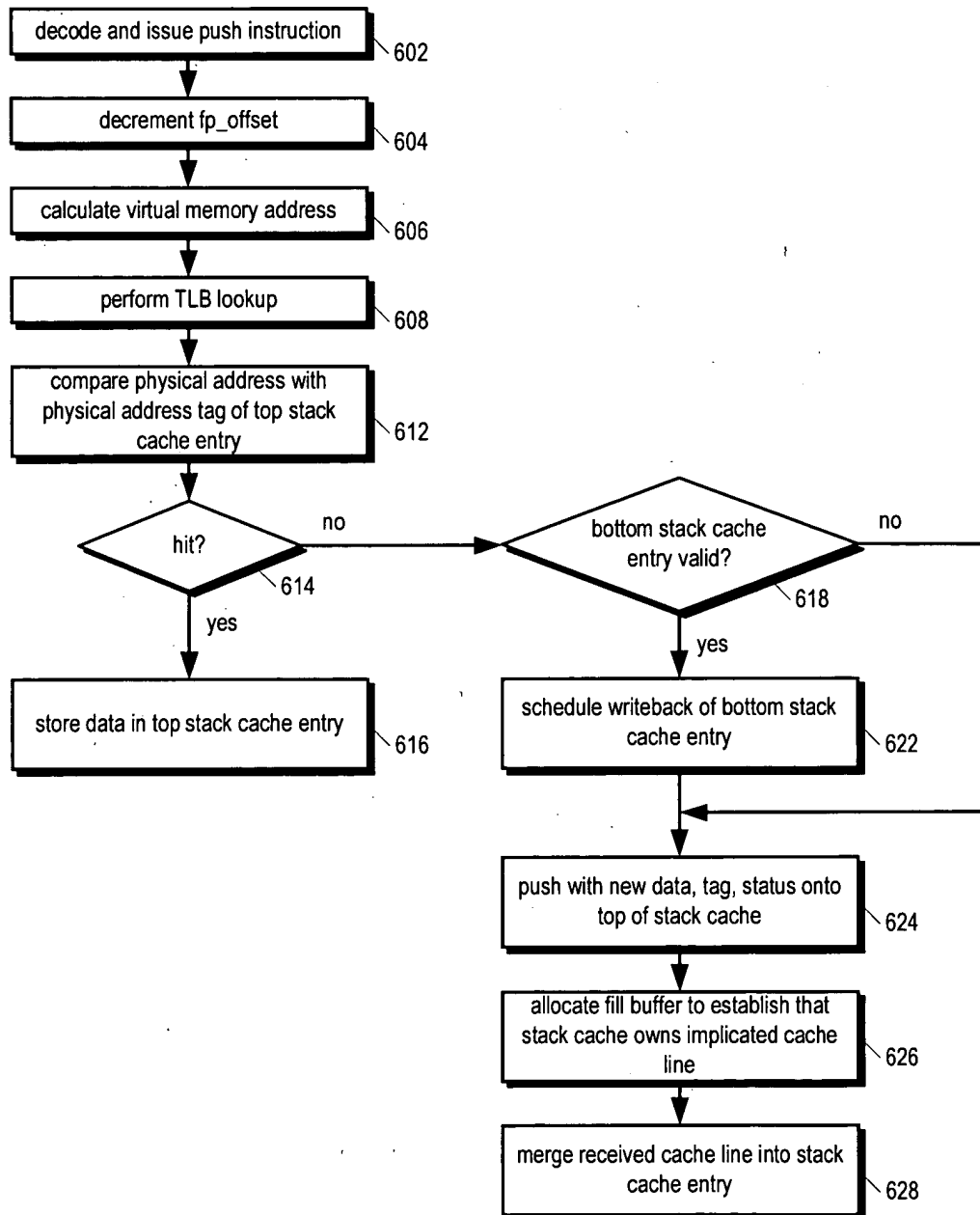
Push Operation

Fig. 7

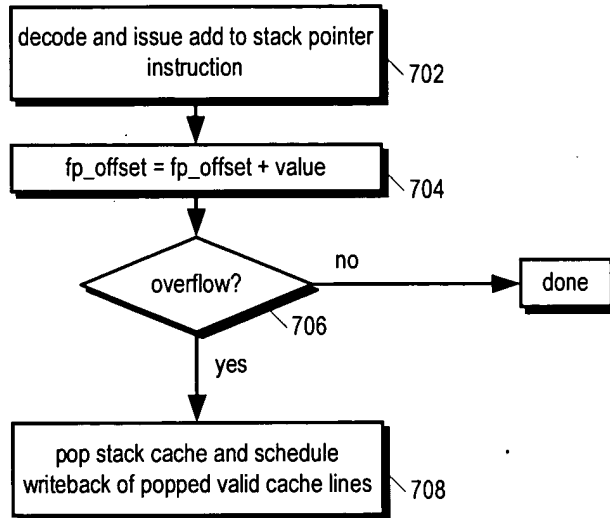
Add to Stack Pointer Operation

Fig. 8A

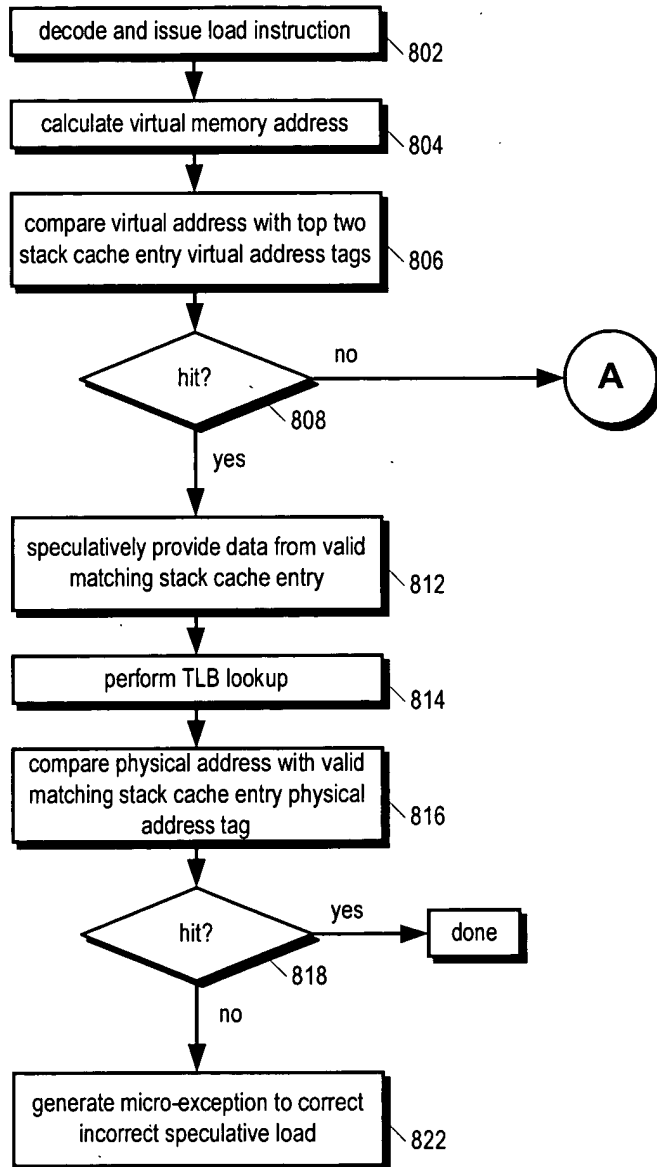
Speculative Load from Stack Cache Operation



Fig. 8B

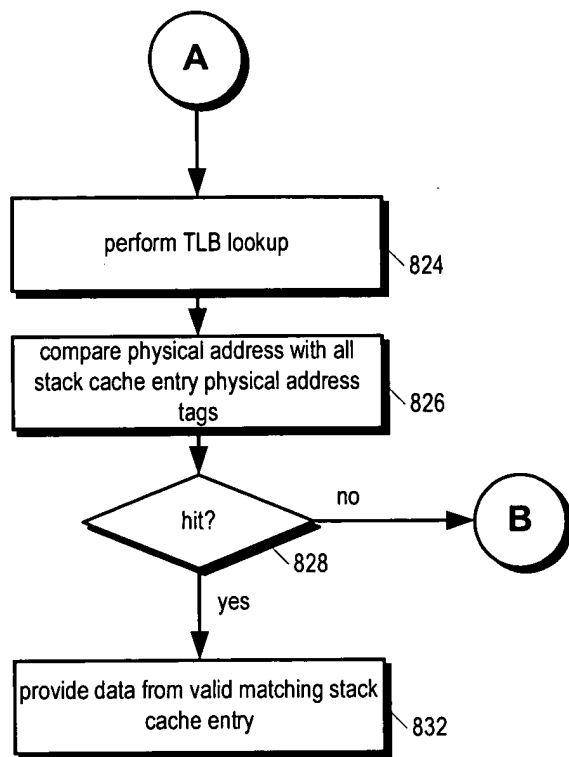
Normal Load from Stack Cache Operation

Fig. 8C

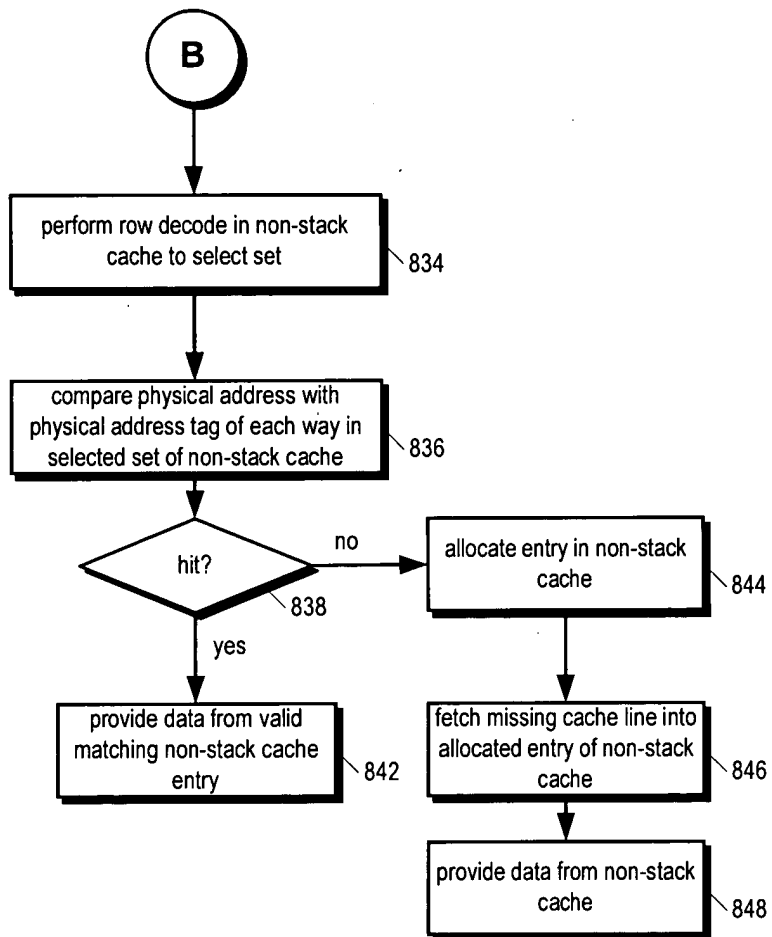
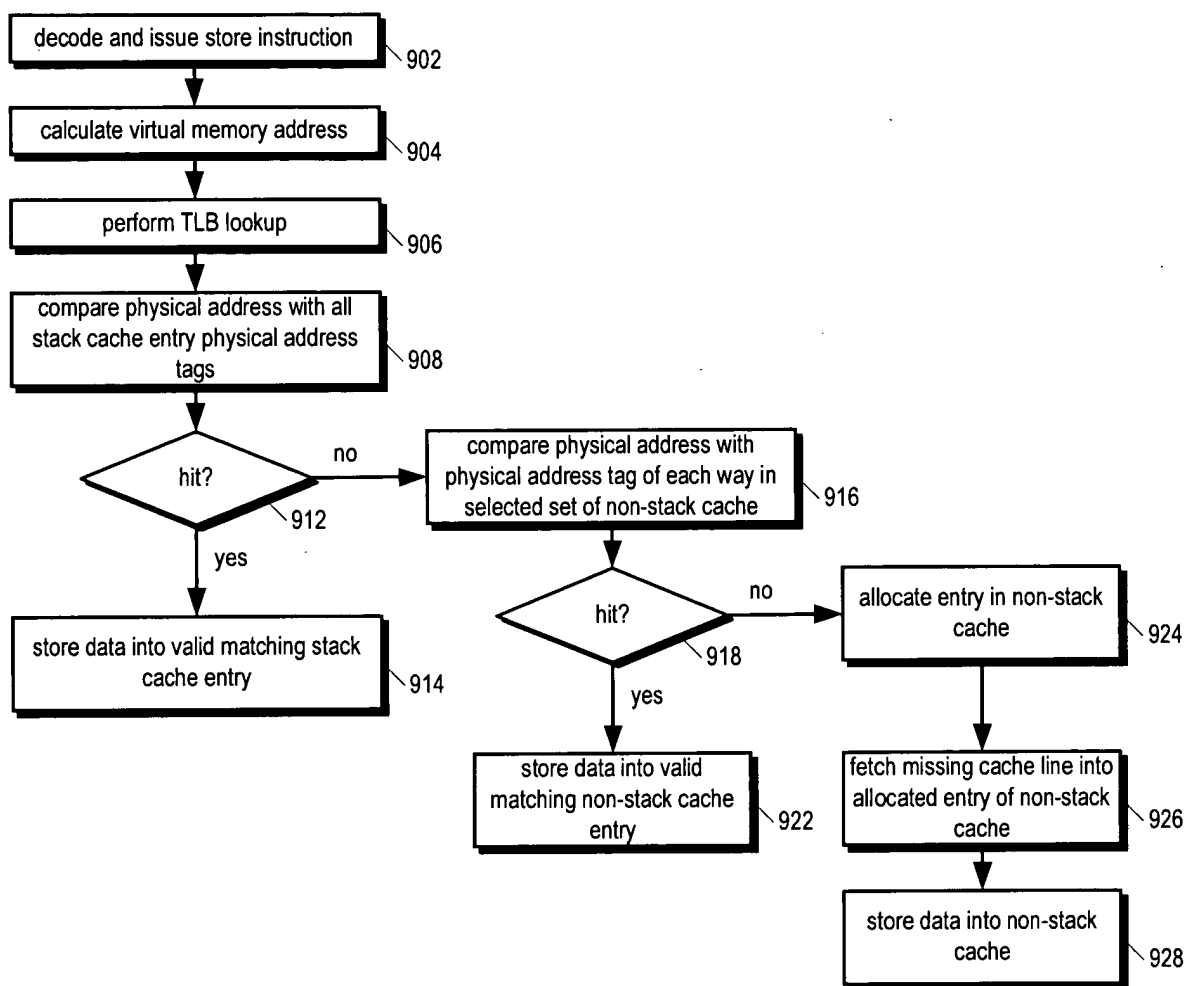
Load from Non-Stack Cache Operation

Fig. 9

Store Operation

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Fig. 10

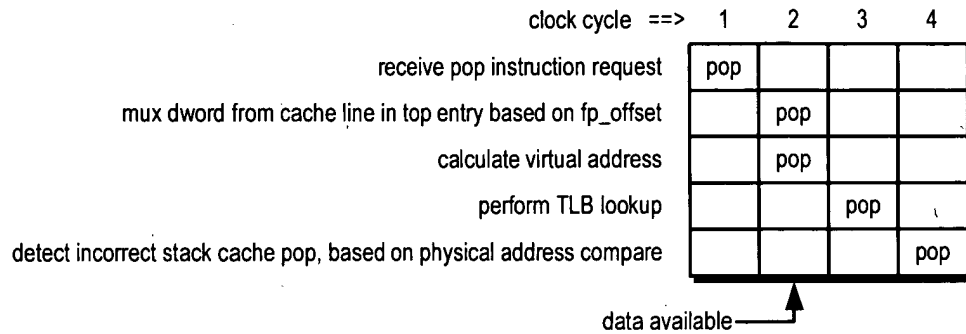
Fast Pop from Stack Cache Timing

Fig. 11

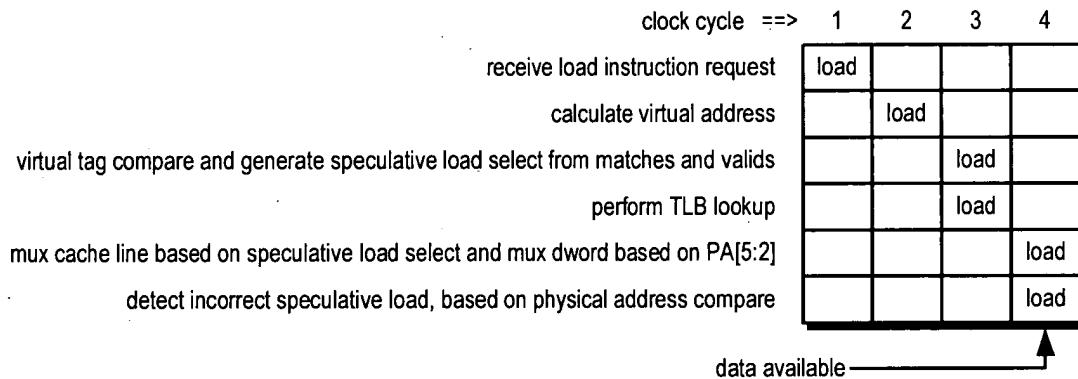
Speculative Load from Stack Cache Timing

Fig. 12

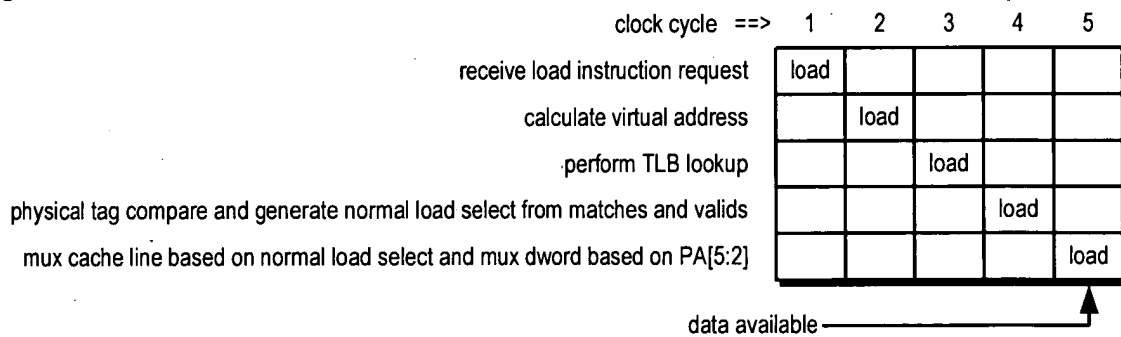
Normal Load from Stack Cache Timing

Fig. 13

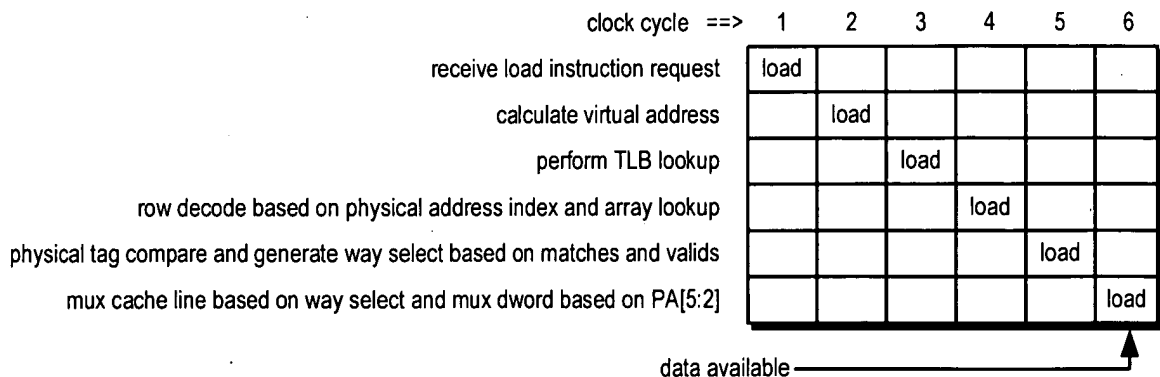
Load from Non-Stack Cache Timing

Fig. 14

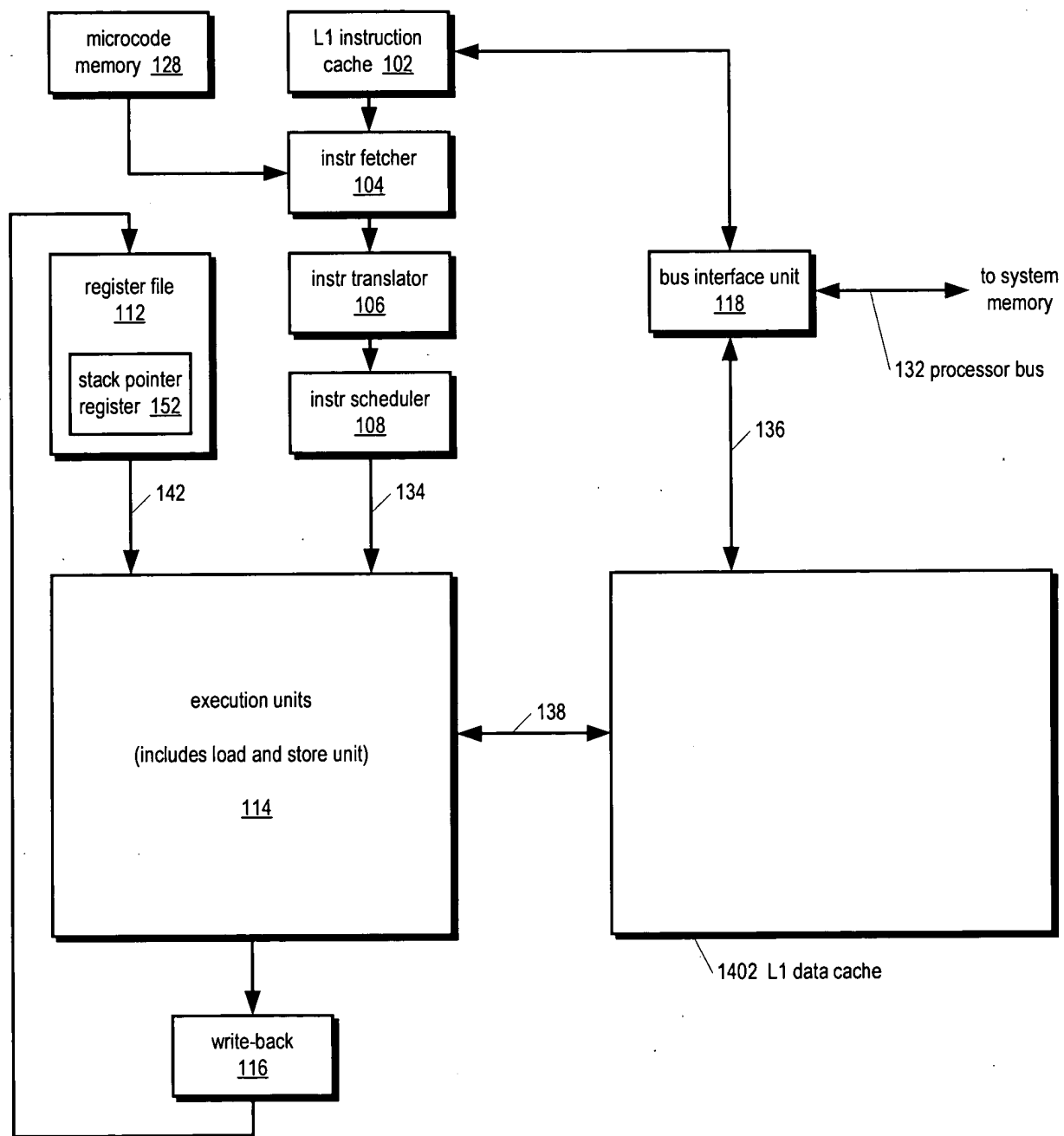
Microprocessor

Fig. 15

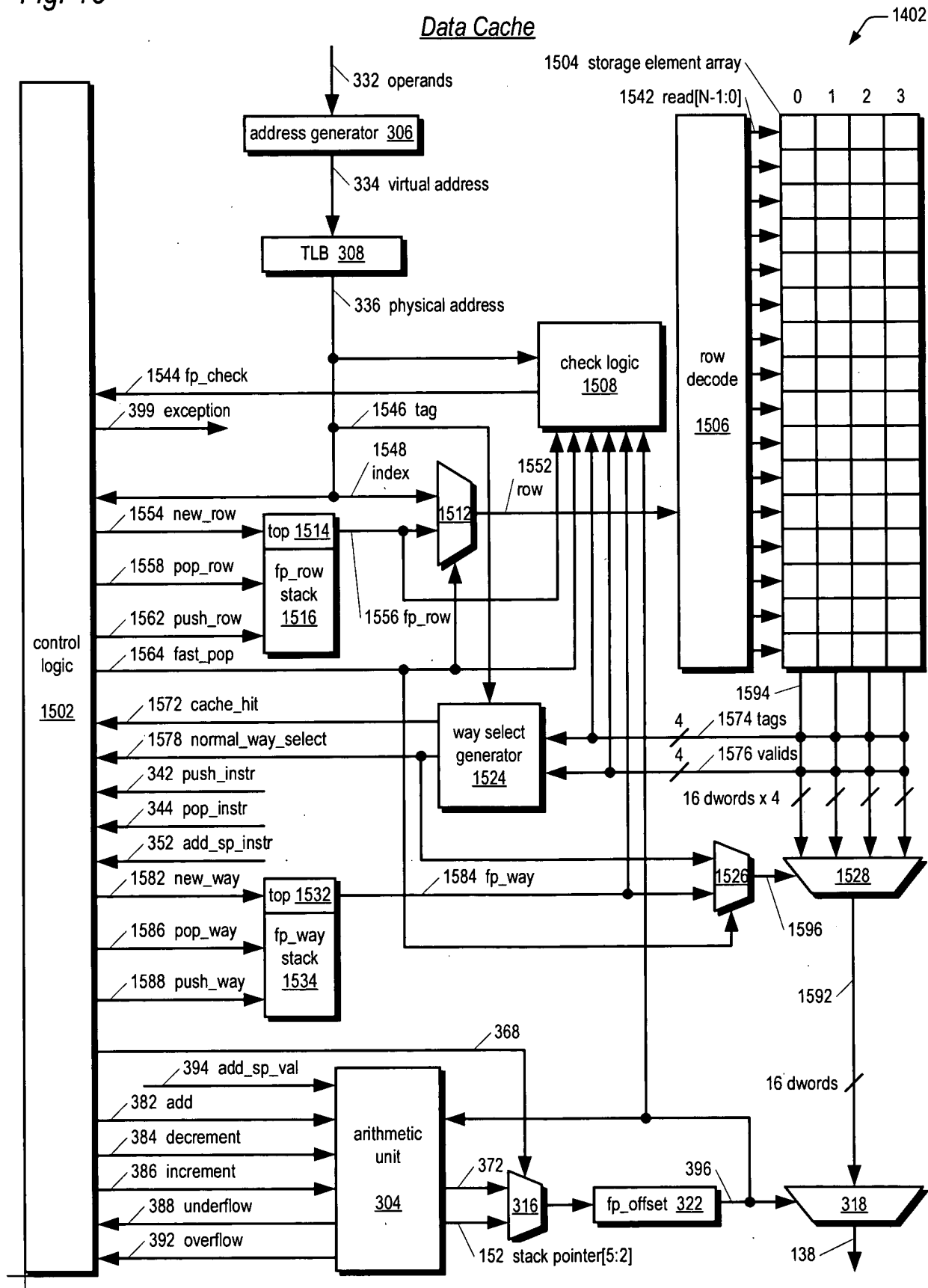


Fig. 16

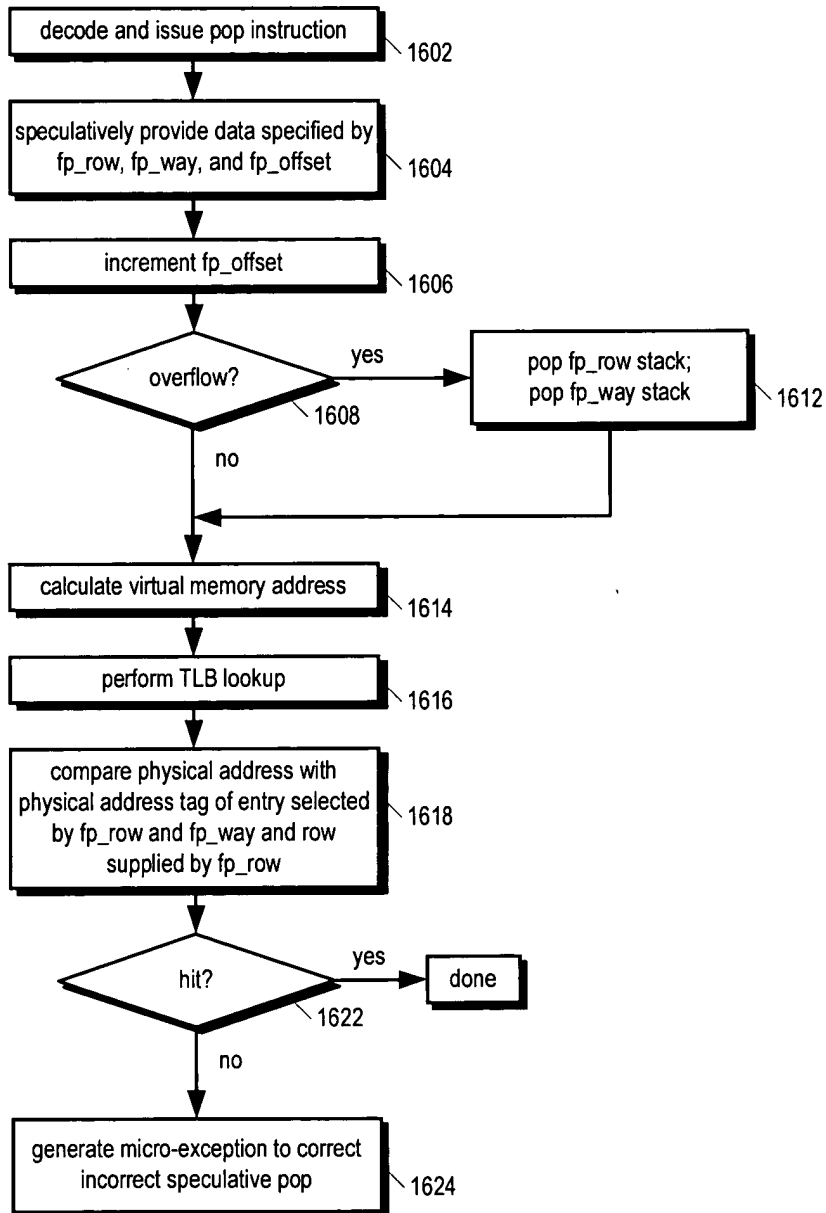
Fast Pop Operation

Fig. 17

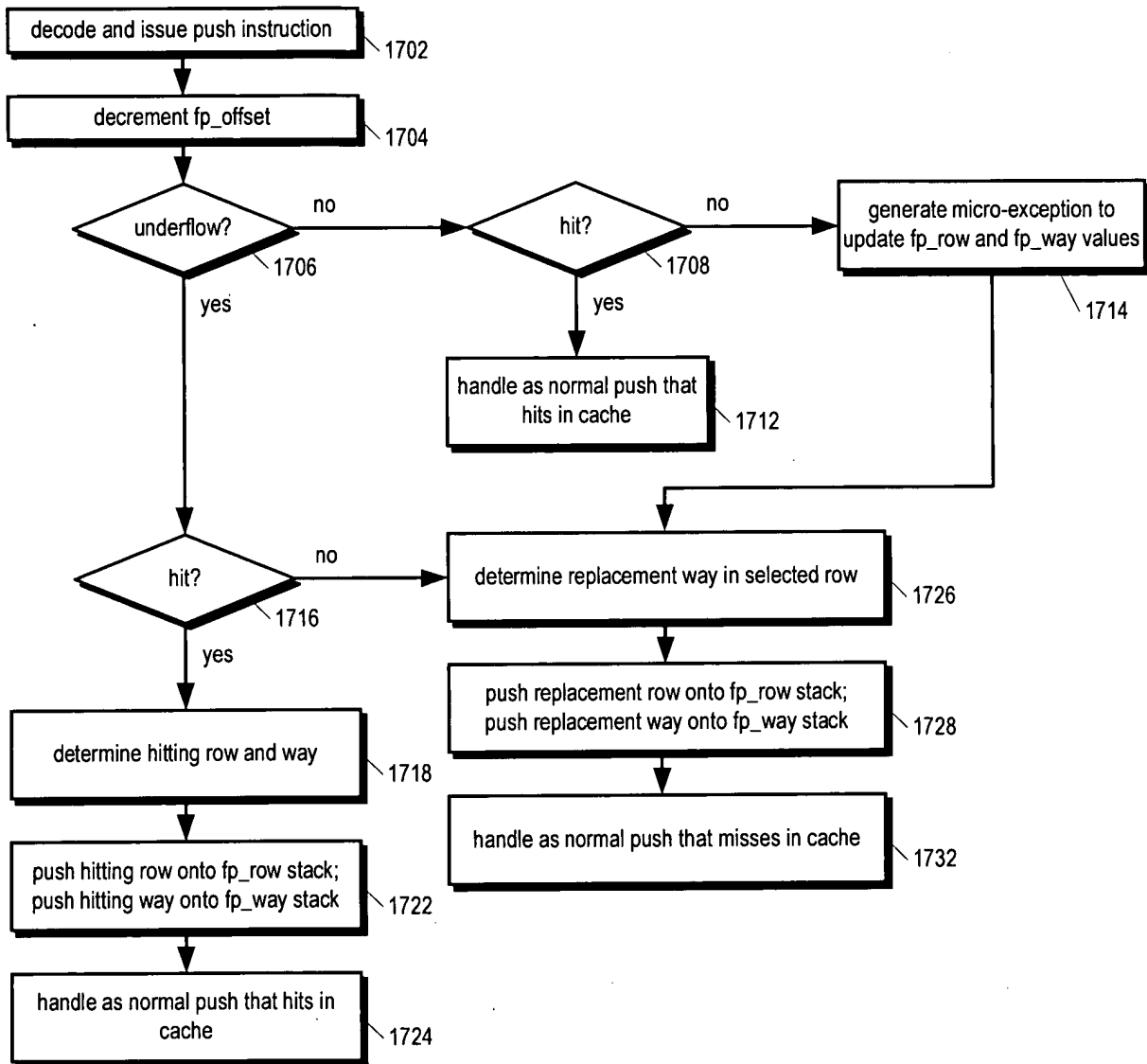
Push Operation



Fig. 18

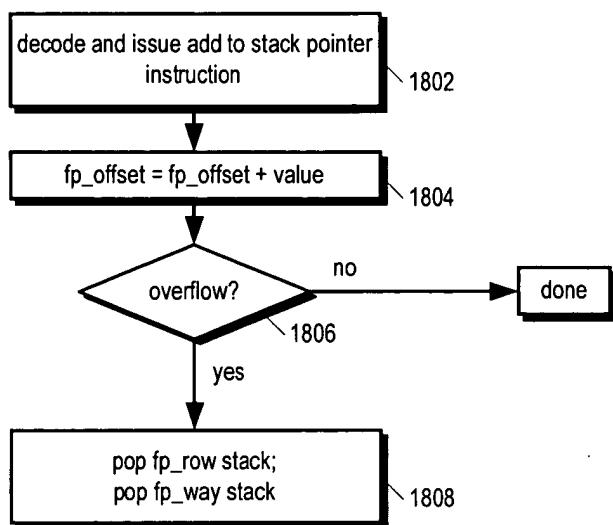
Add to Stack Pointer Operation

Fig. 19

Fast Pop from Cache Timing